(12) UK Patent Application (19) GB (11) 2 350 948 (13) A

(43) Date of A Publication 13.12.2000

(21) Application No 9912873.8

(22) Date of Filing 04.06.1999

(51) INT CL[7]
H04B 1/16 // H03L 7/07 , H04B 1/30

(52) UK CL (Edition R)
H3A AL2D2 AL3X AXX
U1S S2205

(56) Documents Cited
GB 2319913 A EP 0253680 A2 US 4607393 A

(58) Field of Search
UK CL (Edition Q) H3A AB AD AXC AXD AXF AXX
INT CL[6] H03D , H04B

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(54) Abstract Title
Frequency changer and digital tuner

(57) A frequency changer, for example for use in a ZIF digital tuner, comprises multipliers 15 and 16 which receive the RF input signal from an input 1. The multipliers receive quadrature local oscillator signals from a first oscillator 9, 20 of an arrangement which comprises first and second phase-locked loops. The first phase-locked loop comprises a programmable divider 32, a comparator 31 and a control loop 33 so that the first oscillator 9 is phase-locked to a second oscillator 34. A second phase-locked loop comprises the second oscillator 34 and a synthesiser 11 containing a reference oscillator 38 to which the second oscillator 34 is phase-locked. The output frequency of the second oscillator is in a frequency band which is outside the RF input frequency band of the frequency changer.

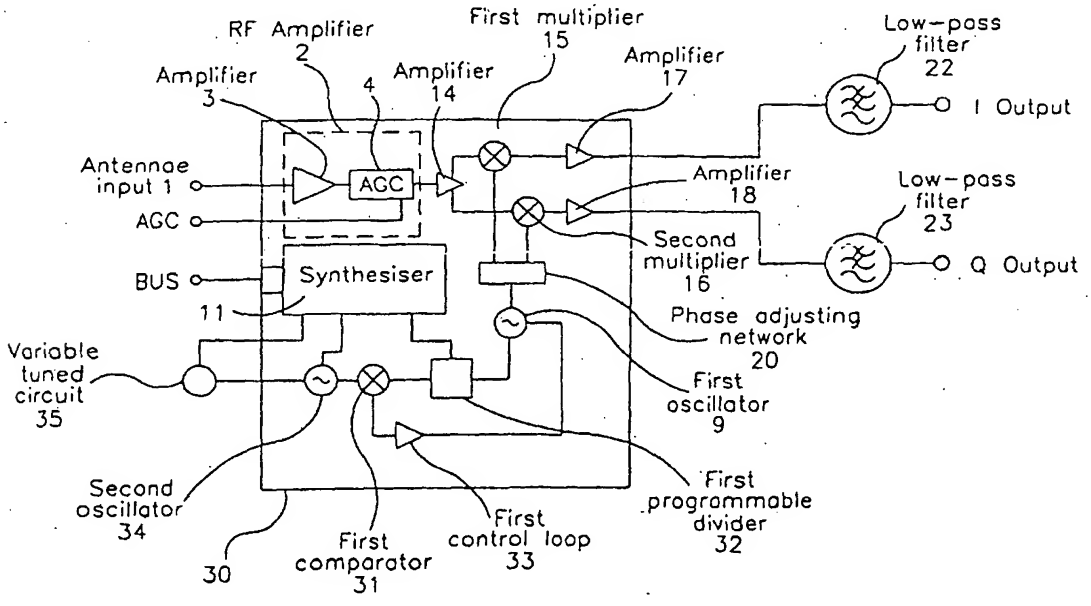

FIG 3

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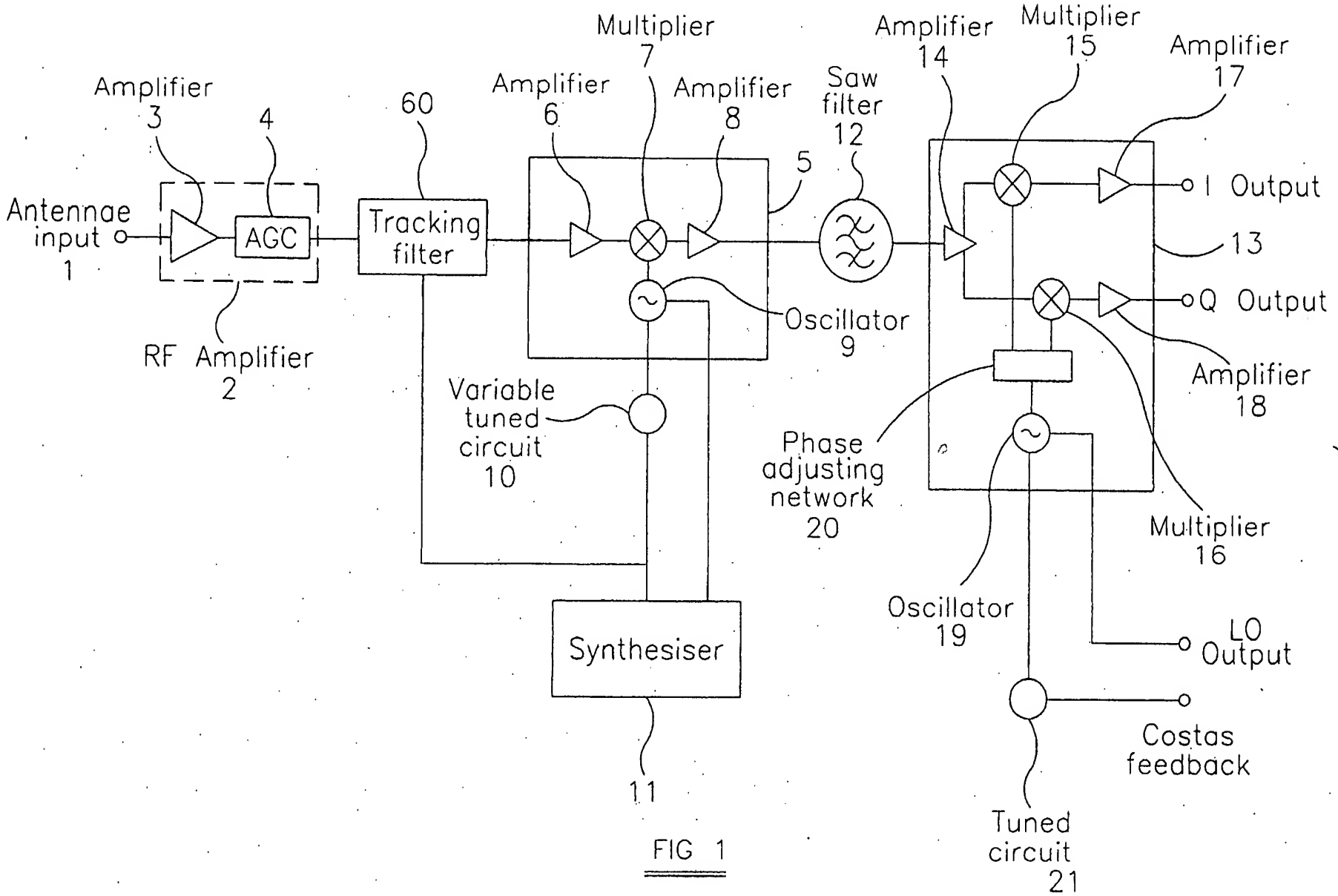

Antennae input 1
Amplifier 3
4
AGC
RF Amplifier 2
60
Tracking filter
Amplifier 6
Multiplier 7
Amplifier 8
5
Oscillator 9
Variable tuned circuit 10
Synthesiser
11
Saw filter 12
Amplifier 14
Multiplier 15
Amplifier 17
I Output
13
Q Output
Amplifier 18
Phase adjusting network 20
Multiplier 16
Oscillator 19
LO Output
Costas feedback
Tuned circuit 21

FIG 1

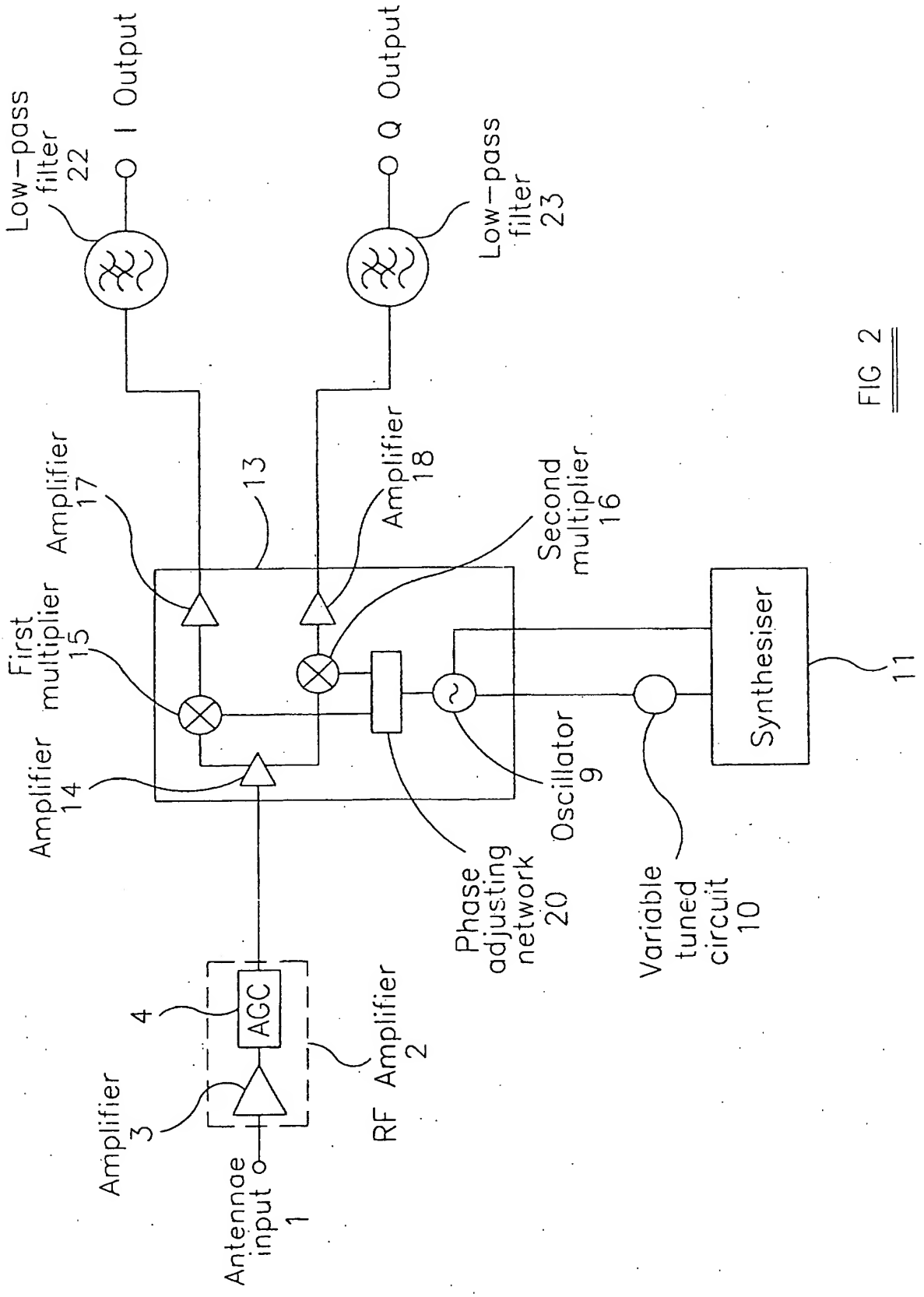

Low-pass filter 22
I Output
Q Output
Low-pass filter 23
Amplifier 17
13
Amplifier 18
First multiplier 15
Second multiplier 16
Amplifier 14
Oscillator 9
Synthesiser 11
Phase adjusting network 20
Variable tuned circuit 10
AGC
4
Amplifier 3
RF Amplifier 2
Antennae input 1

FIG 2

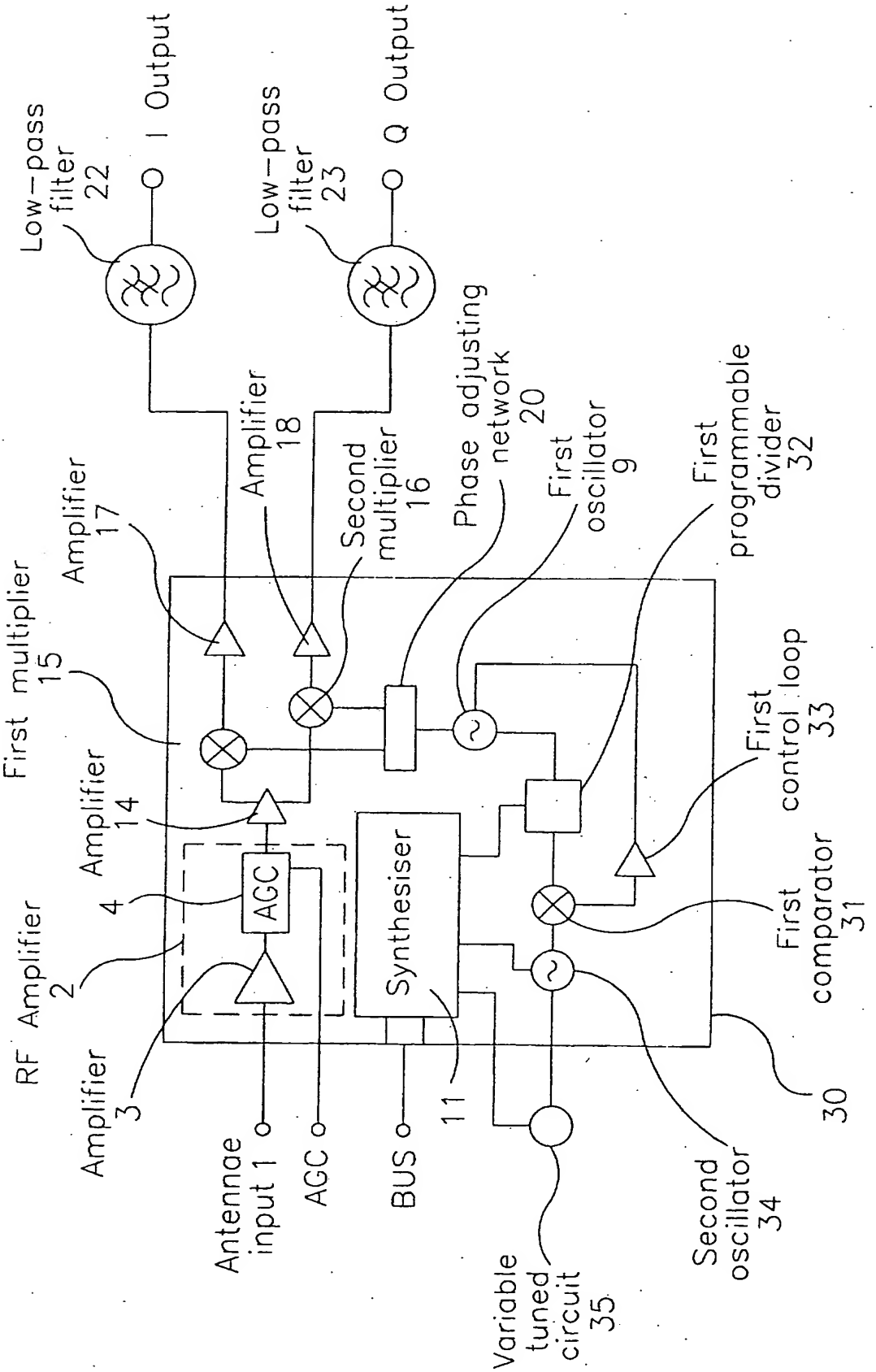

Low-pass filter 22
I Output
Low-pass filter 23
Q Output
Amplifier 18
Second multiplier 16
Phase adjusting network 20
First oscillator 9
First programmable divider 32
First multiplier 15
Amplifier 17
Amplifier 14
First control loop 33
RF Amplifier 2
4
AGC
Synthesiser
First comparator 31
Amplifier 3
Antennae input 1
AGC
BUS
11
30
Second oscillator 34
Variable tuned circuit 35

FIG 3

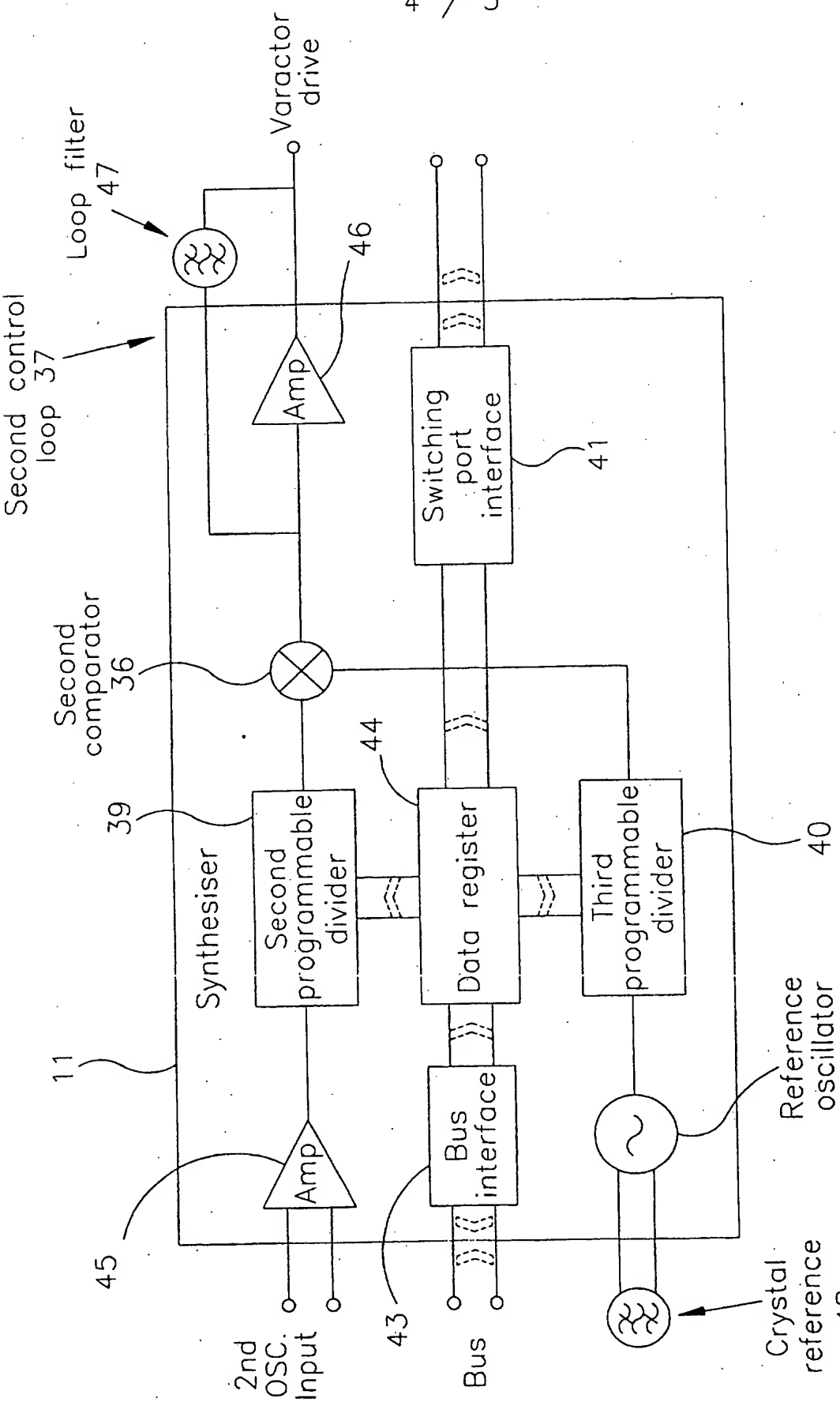
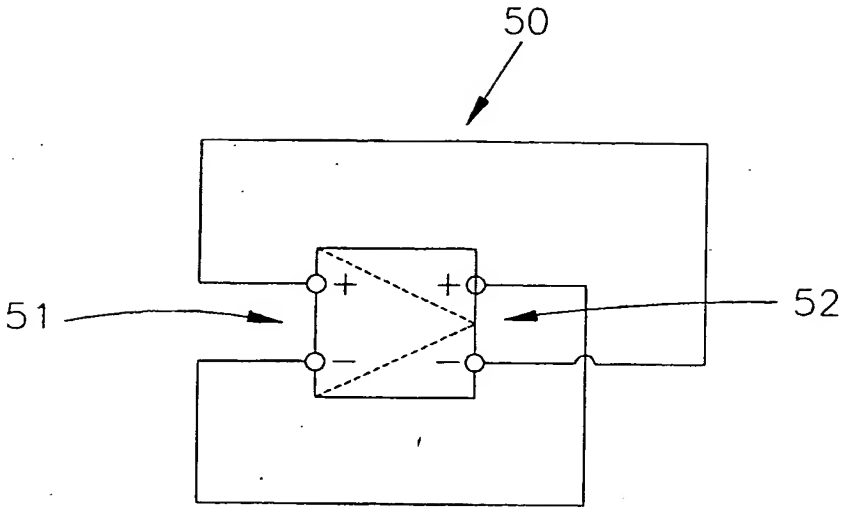

Varactor drive
Loop filter
47
46
Second control loop 37
Amp
Switching port interface
41
Second comparator
36
44
39
Synthesiser
Second programmable divider
Data register
Third programmable divider
40
11
Reference oscillator
38
Amp
Bus interface
45
43
2nd OSC. Input
Bus
Crystal reference
48

FIG 4



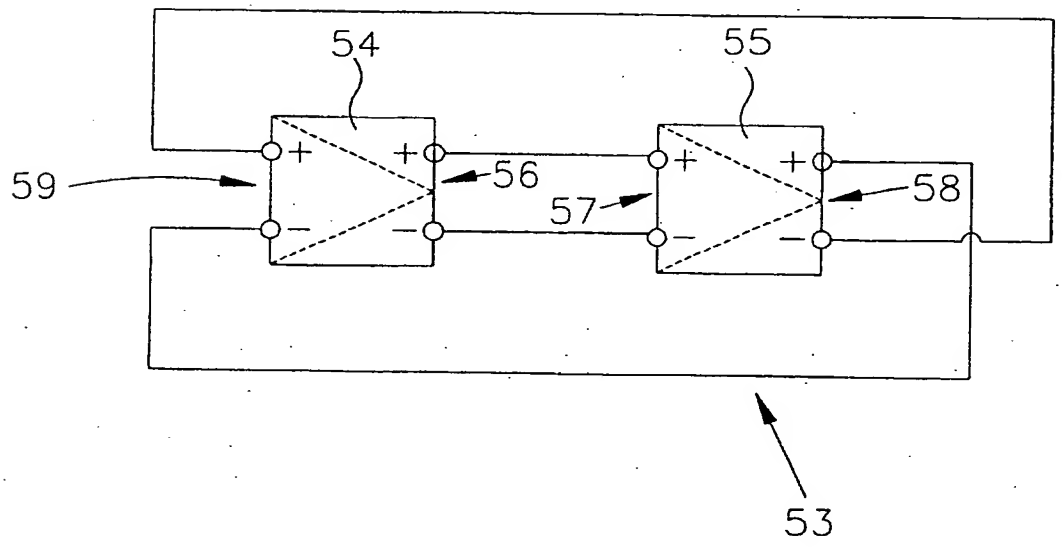


FIG 5

FREQUENCY CHANGER AND DIGITAL TUNER

The present invention relates to a frequency changer. Such a frequency changer may, for example, be used as part of a zero intermediate frequency (ZIF) tuner, for instance, for a digital direct broadcasting by satellite (DBS) receiver system. The present invention also relates to a digital tuner. In general, the invention may be applied to any tuner where a received channel contains a local oscillator frequency.

A known type of digital tuner for use in a DBS system is illustrated in Figure 1 of the accompanying drawings and is based on the well-known super-heterodyning technique, which has been used in analogue tuners for many decades. An antennae input 1 for receiving an input signal from an antennae system is connected to the input of a radio frequency (RF) amplifier 2, which comprises a low noise amplifier 3 and an automatic gain control (AGC) arrangement 4. The RF amplifier 2 is connected to a frequency changer via a tracking bandpass filter 60 tuned to pass the selected channel.

The RF amplifier 2 and the filter 60 form a "front end" which is external to the frequency changer for down-converting the input RF signal to a lower fixed intermediate frequency (IF) which is typically 402 or 480 MHz. The frequency changer comprises a first integrated circuit 5 which comprises an amplifier 6, a multiplier 7, an amplifier 8, and an oscillator 9. The oscillator 9 has an off-chip variable tuned circuit 10 which determines the frequency of oscillation of the oscillator 9 and whose resonant frequency is controlled by a phase-locked loop (PLL) frequency synthesiser 11. The synthesiser 11 also controls tuning of the filter 60, which is offset from the frequency of the oscillator by the IF.

The output of the frequency changer is connected via a bandpass surface acoustic wave (SAW) filter 12 to a quadrature down-converter 13. The down-converter 13 comprises an amplifier 14 which supplies the filtered IF signal to multipliers 15 and 16 whose outputs are connected via amplifiers 17 and 18, respectively, to in-phase (I) and quadrature (Q) outputs. A reference oscillator 19 generates a signal whose frequency is equal to the intermediate frequency. This signal is supplied to the multipliers 15 and 16

via a phase adjusting network 20 so that the multipliers 15 and 16 receive signals which are in quadrature i.e. 90° out of phase which each other.

The oscillator 19 has a frequency-determining tuned circuit 21 which is connected to receive a Costas feedback signal from a Costas de-rotation circuit in a quadrature phase shift keyed (QPSK) demodulator to which the I and Q outputs of the down-converter 13 are connected. Such a demodulator with Costas de-rotation circuitry is well known.

In use, the input signal is amplified and gain-controlled by the RF amplifier 2 and converted by the frequency changer to the IF signal. The synthesiser 11 provides tuning for selecting the frequency of the input signal to be received and demodulated. The down-converter 13 converts the IF signal to base-band in-phase and quadrature output signals which are supplied to the demodulator (not shown). The demodulator supplies the Costas feedback signal to the tuned circuit 21 of the reference oscillator 19 so as to control the phase of the output signal of the oscillator 19 and hence the phases of the quadrature signals supplied to the multipliers 15 and 16. This control loop ensures that the I output supplies the in-phase signal substantially uncontaminated with the quadrature signal whereas the Q output supplies the quadrature signal substantially uncontaminated by the in-phase signal.

Although this known type of digital tuner provides acceptable performance, it is relatively complicated and relatively expensive to manufacture. For example, the parts of the tuner illustrated in Figure 1 have to be fabricated with several integrated circuits and with an external front end and often require alignment of the tracking filter.

Another known type of digital tuner for use in DBS receivers differs from that illustrated in Figure 1 in that the de-rotation function is performed by subsequent digital signal processing (DSP) techniques. The Costas feedback signal to the tuned circuit 21 is thus unnecessary and the reference oscillator 19 is free-running i.e. not phase-locked. The output signals from the amplifiers 17 and 18 each therefore contain both in-phase and quadrature signals which are subsequently extracted by digital signal processing.

Figure 2 of the accompanying drawings illustrates another known type of digital tuner for use in a DBS receiving system. The tuner is of the ZIF type and converts the input signal in a single conversion step to the base-band signals. The tuner illustrated in Figure 2 differs from that illustrated in Figure 1 in that the frequency changer and down-converter are combined into a single frequency changer stage 13, which comprises the amplifiers 14, 17, 18 and multipliers 15 and 16 with the oscillator 9, the variable tuned circuit 10 and the synthesiser 11. The bandpass filter 12 is eliminated and the I and Q outputs are supplied via low-pass filters 22 and 23.

The frequency of the oscillator 9 set by the synthesiser 11 is at or very near the centre frequency of the channel containing the desired input signal as supplied by the RF amplifier 2. Local oscillator signals are supplied in quadrature by the phase adjusting network 20 to the first and second multipliers 15 and 16, which supply base-band demodulated signals via the low-pass filters 22 and 23 to subsequent digital signal processing circuitry for performing de-rotation to retrieve the orthogonal in-phase and quadrature modulation signals.

Although the ZIF tuner shown in Figure 2 represents a substantial simplification compared with the tuner shown in Figure 1, it is still not possible to form all of the main tuner circuitry in a single integrated circuit and achieve the necessary performance for acceptable results.

The problems with such a tuner architecture result from the fact that the local oscillator frequency in the frequency changer 13 is within the frequency band or channel of the desired input signal. Because the two signals are of substantially the same frequency, any signal leakage which inevitably occurs results in interference between the signals as explained below.

Leakage of the local oscillator signal to the RF input has two effects. First, such leakage results in re-radiation of the local oscillator signal to other tuners which may be connected to the same antenna system or maybe located nearby. Although this problem may be substantially overcome by providing an external front end as illustrated at 2 in

Figure 2 having sufficient "reverse isolation" to meet tuner re-radiation specification requirements, it is then impossible to provide an "internal" RF amplifier 2, for example within the integrated circuit in which the main parts of the frequency changer 13 are formed.

Second, local oscillator signals leaking to the input are amplified and supplied with the input signal to the frequency changer 13. Because of phase shifts which are inherent in such leakage mechanisms and because of amplification within the ZIF tuner, this results in a DC imbalance at the outputs of the frequency changer 13. Such a DC imbalance can represent a significant fraction of the desired signal and cannot be improved because of limits to the degree of isolation which is achievable.

Leakage also occurs from the RF input to the local oscillator and this results in "injection pulling" of the local oscillator 9. This in turn degrades the phase noise and hence the quality of the signal supplied by the oscillator 9 to the multipliers 15 and 16, resulting in reduced signal-to-noise performance of the tuner. Injection pulling results from the injection of the RF signal into the oscillator, which is in effect a tuned amplifier with a low Q feedback network at the oscillation frequency. The injected RF signal is amplified within the oscillator loop and effectively impresses its characteristic on the output of the reference oscillator 9. The RF signal carries a pseudo random noise (PSRN) type modulation and appears like broadband noise, which is impressed on the oscillator signal and thus degrades the noise performance.

The degradation caused by injection pulling to the oscillator phase noise performance thus limits the application of ZIF techniques within DBS applications because lower data rates require a very pure local oscillator signal in order to achieve satisfactory performance. In practice, in order to achieve satisfactory performance with ZIF techniques, a relatively low amplitude input signal must be supplied to the input of the ZIF circuit and this results in disadvantages such as reduced dynamic range. Alternatively or additionally, complex techniques must be used in order to suppress injection pulling so as to achieve the desired standard of performance.

It is known in other applications to form the reference oscillator "on chip" so as to reduce oscillator coupling, for which the dominant leakage mechanism is through parasitic components in integrated circuit packaging and by electromagnetic coupling to and from oscillator strip lines. Such techniques have been used, for example, in global positioning satellite (GPS) receiver systems, for example as disclosed in Schaeffer Shahani et al, "A 115 mW CMOS GPS Receiver", ISSCC98 paper Ref. FA 8.1. However, such integrated oscillators have such inherently poor phase noise characteristics that they are totally unsuitable for use in DBS receiving systems. Also, such techniques have been applied to conventional super-heterodyning architectures but have not been applied to ZIF architectures.

It is well-known that an oscillator with poor phase noise performance can be improved by applying a phase-locked loop to control the phase noise within the loop bandwidth. Such techniques are, for example, disclosed in "Digital PLL Frequency Synthesisers", Rohde, Prentice Hall, 1983, ISBN 013 214 293-2. However, this provides no improvement in phase noise outside the loop bandwidth. The maximum loop bandwidth which may be applied is determined by the required reference oscillator frequency step size and is of the order of a few kilohertz. Thus, the integrated phase noise outside this bandwidth has a significant detrimental effect on performance.

According to the invention, there is provided a frequency changer as defined in the appended claim 1.

Preferred embodiments of the invention are defined in the other appended claims.

Such arrangements provide substantial improvements in tuner performance, for example making substantially fully integrated ZIF tuners with acceptable performance a practical possibility. The second oscillator can be phase-locked, for example by a low noise PLL frequency synthesiser incorporating the reference oscillator, and so has very good phase noise performance because it can be required to tune over a relatively narrow frequency range and hence have a high Q. By phase-locking the first oscillator to the second oscillator, the resulting local oscillator signal for mixing or multiplying with the input

signal has very low phase noise and is resistant to injection pulling. For example, the feedback bandwidth of the control loop for the first oscillator can be arranged to be high enough to cover the bandwidth of the input signal so that the free-running phase noise of the first oscillator is greatly reduced by the phase-locking to the second oscillator. It is thus possible to provide, for example, a ZIF digital tuner which is suitable for DBS applications and which can be formed as a single monolithic integrated circuit with very few external or off-chip components.

The present invention will be further described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block circuit diagram of a first known type of digital tuner;

Figure 2 is a block circuit diagram of a second known type of digital tuner;

Figure 3 is a block circuit diagram of a digital tuner and frequency changer constituting an embodiment of the invention;

Figure 4 is a block circuit diagram of a synthesiser of the tuner shown in Figure 3; and

Figure 5 is a schematic diagram illustrating a single-stage oscillator and a ring oscillator which may be used in the frequency changer shown in Figure 3.

Like reference numerals refer to like parts throughout the drawings.

The digital tuner and frequency changer shown in Figure 3 comprise a ZIF tuner for receiving and demodulating QPSK signals, for example in a DBS receiver system. The tuner receives input signals in an input frequency band which is typically from 950 to 2150 MHz. A plurality of channels are located within this input band, for example having centre frequencies which are equally spaced, for example at the Nyquist bandwidth.

The tuner effectively comprises a frequency changer in the form of a single monolithic integrated circuit 30 with very few external components. The frequency changer is of the ZIF type and is similar to that shown in Figure 2. Accordingly, those elements and components of the tuner shown in Figure 3 which are the same as the corresponding elements and components shown in Figure 2 will not be described again in detail.

The frequency changer 30 includes the RF amplifier 2 within the integrated circuit and has an AGC input for receiving a control voltage from an arrangement of known type (not shown) for controlling the gain of the RF amplifier 2 so as to present to the amplifier 14 input signals of substantially constant maximum amplitude substantially irrespective, within the gain control range, of the amplitude of input signals supplied to the antenna input 1.

The first oscillator 9 generates a local oscillator signal which is supplied in quadrature by the phase adjusting network 20 to the first and second multipliers 15 and 16. The synthesiser 11 has a BUS input for selecting the desired input channel and controls the oscillator arrangement including the first oscillator 9 so that the signals supplied by the first oscillator 9 have a frequency which can be tuned within the input frequency band of 950 to 2150 MHz.

The first oscillator 9 forms part of a phase-locked loop which comprises a first comparator 31, a first programmable divider 32 and a first control loop 33. The first programmable divider 32 has a division ratio or divisor which is selectable by the BUS signals to be 2,3 or 4. The output signal of the first oscillator 9 is divided by the divisor selected in the divider 32 and supplied to one input of the first comparator 31, whose other input receives signals from a second oscillator 34. The first comparator 31 comprises a frequency/phase comparator which forms an error signal for driving the first control loop 33, which comprises an amplifier and loop filter whose bandwidth is at least as large as the bandwidth of the input signals supplied to the antenna input 1. The amplified and filtered feedback signal is supplied to a frequency control input of the first oscillator 9, whose output frequency is therefore twice, three times or four times the frequency of the output signal of the second oscillator 34. The phase noise of the

first oscillator 9 within the control loop bandwidth is therefore substantially determined by the phase noise performance of the second oscillator 34. Thus, the first oscillator 9 is substantially immune to injection pulling.

Because the first oscillator 9 is located in the integrated circuit forming the frequency changer 30, signal leakage is substantially reduced. The performance of the amplifier 3 is such that local oscillator leakage to the input 1 can be substantially reduced so that re-radiation interference to other tuners connected to the antenna system can be reduced to acceptable limits. Similarly, leakage of local oscillator signals to the frequency changer input is at a sufficiently low level to avoid significant DC shifting of the I and Q outputs. Further, the immunity to injection pulling allows the full unattenuated signal to be supplied to the amplifier 3 and later stages so that the dynamic range performance of the frequency changer does not need to be compromised in order to avoid or reduce injection pulling.

The second oscillator 34 has a frequency range which is typically 400 to 600 MHz within the UHF band. The frequency of oscillation is determined by a variable tuned circuit 35, for example of the varactor diode tuned type, which is located externally to the integrated circuit 30 ("off-chip"). The second oscillator 34 forms part of a second phase-locked loop which, as shown in Figure 4, also comprises the main elements of the synthesiser 11. In particular, the second phase-locked loop comprises the second oscillator 34, a second comparator 36, a second control loop 37, a reference oscillator 38, and second and third programmable dividers 39 and 40. In addition, the synthesiser 11 comprises a data register 44 for supplying control signals for setting the division ratios or divisors of the second and third programmable dividers 39 and 40 and for setting via a switching port interface 41 the divisor in the first programmable divider 32. A BUS interface 43 provides interfacing between the input BUS and the data register 44.

The output of the second oscillator 34 is connected via an input and an amplifier 45 to the second programmable divider 39 which divides the frequency by a divisor as set by the data register 44 and supplies the resulting frequency-divided signal to one input of

the second comparator 36, which operates as a frequency/phase comparator. The other input of the comparator 36 receives the reference oscillator output signal via the programmable divider 40 which likewise divides the frequency in accordance with a divisor as set by the data register 44. The second comparator 36 produces an output signal which is supplied via the second control loop 37, which comprises an amplifier 46 and a loop filter 47, to the variable tuned circuit 35. The reference oscillator 38 is provided with a crystal reference tuned circuit 48 such that the output frequency of the reference oscillator 38 is fixed to very high stability and the reference oscillator 38 produces very low phase noise.

The phase noise of the second oscillator 34 is effectively determined by the phase noise of the reference oscillator 38 within the bandwidth of the loop filter 47. The crystal-controlled reference oscillator 38 has very low phase noise and the bandwidth of the loop filter 47 is such that the second oscillator 34 has very low phase noise within its loop bandwidth, for example up to a few kilohertz. Thus, the phase noise of the first oscillator 9 is correspondingly low and the first oscillator 9, as described hereinbefore, is substantially immune to injection pulling. This provides the frequency changer and tuner with a very good signal/noise ratio.

The outputs of the frequency changer are supplied via the low-pass filters 22 and 23 which have a cut-off frequency appropriate to the modulation spectrum of the input signals. For example, for typical DSB receiver systems, the cut-off frequency of the filters 22 and 23 is between 5 and 40 MHz.

It is thus possible to provide a digital tuner of the ZIF type in which virtually the whole of the frequency changer can be embodied as a single monolithic integrated circuit. The additional circuitry, for example as compared with the frequency changer shown in Figure 2, does not significantly increase the complexity of the integrated circuit, which can therefore be easily manufactured without substantial cost penalties. Further, the RF amplifier can be incorporated in the integrated circuit without degradation in performance due to leakage, in particular between the RF input and the local oscillator

and vice versa. Thus, injection pulling effects and in-hand local oscillator leakage effects can be greatly reduced or even substantially eliminated.

As shown in Figure 3, the quadrature local oscillator signals required by the first and second multipliers 15 and 16 can be supplied by a single-phase oscillator 9 and a phase adjusting network 20. An alternative oscillator arrangement for generating quadrature local oscillator signals without requiring the phase adjusting network 20 is illustrated in Figure 5. A conventional oscillator is illustrated schematically at 50 in Figure 5 and essentially comprises a single gain stage with 180° feedback between the input 51 and the output 52. This arrangement provides a single-phase output signal from the output 52. A ring oscillator is illustrated schematically at 53 and comprises two identical gain stages 54 and 55. The output 56 of the first stage is connected to the input 57 of the second stage 55 with 180° feedback from the output 58 of the second stage 55 to the input 59 of the first stage 54.

In use, the total phase shift across the two identical gain stages 54 and 55 is substantially equal to 180°. Accordingly, the phase shift across each of the stages 54 and 55 is 90°. Thus, the outputs 56 and 58 of the stages 54 and 55 produce local oscillator signals which are accurately in quadrature with each other and which may therefore be supplied directly to the first and second multipliers 15 and 16.

CLAIMS:

1. A frequency changer comprising a first multiplier having a first input for receiving an input signal in an input frequency band and a second input connected to an oscillator arrangement, which comprises a first oscillator for supplying a first signal in a first frequency band to the second input of the multiplier, a second oscillator for producing a second signal in a second frequency band outside the input frequency band, and a reference oscillator, the first oscillator being phase-locked to the second oscillator and the second oscillator being phase-locked to the reference oscillator.

2. A frequency changer as claimed in claim 1, in which the second frequency band is lower than the first frequency band.

3. A frequency changer as claimed in claim 1 or 2, in which the first frequency band is within or substantially equal to 950 to 2150 MHz.

4. A frequency changer as claimed in any one of the preceding claims, in which the second frequency band is within the UHF band.

5. A frequency changer as claimed in claim 4, in which the second frequency band is within or substantially equal to 400 to 600 MHz.

6. A frequency changer as claimed in any one of the preceding claims of the zero or near zero intermediate frequency type, in which the first frequency band is equal to the input frequency band.

7. A frequency changer as claimed in claim 6, in which the multiplier has an output for supplying an output signal to a low pass filter.

8. A frequency changer as claimed in claim 7, in which the low pass filter has a cut-off frequency of between 5 MHz and 40 MHz.

9. A frequency changer as claimed in any one the preceding claims, comprising a second multiplier having a first input for receiving the input signal and a second input connected to the oscillator arrangement for receiving a quadrature signal which is in quadrature with the first signal.

10. A frequency changer as claimed in claim 9, in which the first oscillator is connected to a phase adjusting network for forming the first signal and the quadrature signal.

11. A frequency changer as claimed in claim 9, in which the first oscillator comprises a ring oscillator having first and second outputs for supplying the first signal and the quadrature signal.

12. A frequency changer as claimed in any one of the preceding claims, in which the first and second oscillators form part of a first phase-locked loop comprising a first programmable divider, a first comparator having a first input connected via the first divider to the first oscillator and a second input connected to the second oscillator, and a first control loop connected between the output of the first comparator and a control input of the first oscillator.

13. A frequency changer as claimed in claim 12, in which the first programmable divider has selectable divisors of two, three and four.

14. A frequency changer as claimed in any one of the preceding claims, in which the second and reference oscillators form part of a second phase-locked loop comprising: a second comparator having a first input connected via a second programmable divider to the second oscillator and a second input connected via a third programmable divider to the reference oscillator; and a second control loop connected between the output of the second comparator and a control input of the second oscillator.

15. A frequency changer as claimed in any one of the preceding claims, in which the first multiplier and the oscillator arrangement are formed in a monolithic integrated circuit.

16. A frequency changer as claimed in claim 15 when dependent on claim 9, in which the second multiplier is formed in the integrated circuit.

17. A frequency changer as claimed in claim 15 or 16 when dependent on claim 12, in which the first phase-locked loop is formed in the integrated circuit.

18. A frequency changer as claimed in any one of the claims 15 to 17 when dependent on claim 14, in which the second phase-locked loop is formed in the integrated circuit.

19. A frequency changer as claimed in any one of claims 15 to 18, in which the second oscillator comprises a frequency-determining resonant circuit disposed externally of the integrated circuit.

20. A frequency changer as claimed in any one of claims 15 to 18, comprising an amplifier connected between the first input of the first multiplier and an input terminal and formed in the integrated circuit.

21. A frequency changer as claimed in claim 20, in which the amplifier has a controllable gain for providing automatic gain control.

22. A digital tuner comprising a frequency changer as claimed in any one of the preceding claims.

The Patent Office

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INVESTOR IN PEOPLE

Application No: GB 9912873.8 **Examiner:** Mr.Sat Satkurunath
Claims searched: ALL **Date of search:** 1 July 1999

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H3A: AB, AD, AXC, AXD, AXF, AXX

Int Cl (Ed.6): H03D, H04B

Other:

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2319913 A	NEC - see especially figures 4b, 4c	1, 2
X	EP 0253680 A2	NIPPON -see especially figures 2, 3	1, 2
X	US 4607393	NOLDE - see especially figure 1 and abstract	1, 2

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.